A Novel Readout Scheme with Controllable Delay Chains for High-Precision Time Resolution in Pixel Detectors*

Ni Fang,[1] Dong Wang,[1,†] Zhuo Zhou,[1] Ran Chen,[1] Shi-Qiang Zhou,[1] Hui Wang,[1] Chun-Lai Dong,[1] and Fan Zhang[2]

[1]*PLAC, Key Laboratory of Quark & Lepton Physics (MOE), Central China Normal University, Wuhan 430079, China*

[2]*Hubei Collaborative Innovation Center for High-efficiency Utilization of Solar Energy, Hubei University of Technology, Wuhan, 430068, China.*

With the widespread application of pixel detectors in particle physics, imaging technologies, and other high-precision fields, improving time resolution and signal processing speed has become a critical challenge. Traditional readout schemes face a trade-off between precision and processing efficiency, highlighting the need for innovative solutions. This study presents a novel readout scheme for pixel detectors, aimed at enhancing time resolution and response speed to meet the demands of particle information reconstruction and real-time data analysis. The scheme uses controllable delay chains to facilitate multi-directional signal propagation, enabling precise particle localization based on differences in transmission paths, which in turn enhances the readout system's time resolution. Each pixel circuit integrates a low-noise charge-sensitive amplifier, a comparator, and a controllable delay unit, which together enable precise signal processing. Based on the TSMC 180 nm process, two transmission configurations are proposed: a four-directional delay chain configuration (ASIC-I) and a two-directional delay chain configuration (ASIC-II). These configurations address different signal propagation needs, further improving time resolution. Experimental results show that the ASIC-I chip, with a 3 × 3 pixel array, achieves a single-pixel delay precision of 108.5 ps, a delay range of 4.55 ns to 31.10 ns (7 levels), and a time resolution of 160 ps. Stability tests under varying PVT (process, voltage, and temperature) conditions confirm the design's robustness, with a temperature coefficient ranging from 7 ps/°C to 44 ps/°C. These results validate the robustness and reliability of the proposed scheme for practical applications.

Keywords: charge-sensitive amplifier, delay chain, pixel detectors, PVT, time resolution

I. INTRODUCTION

In fields such as high-energy physics experiments, astronomy, and medical imaging, pixel detectors serve as a core component, with their high-precision temporal and spatial resolution being crucial for accurate particle trajectory and energy measurements[1–6]. As the performance requirements for detectors in these areas continue to increase[7–9], traditional readout schemes face bottlenecks in response speed and time resolution, especially in complex noise environments[10, 11], making it increasingly difficult to maintain high precision and efficient signal processing. In recent years, significant progress has been made in pixel detectors by reducing pixel sizes and utilizing high-speed in-pixel readout circuits. However, many technical challenges remain[12, 13]. For instance, in the ALICE experiment at CERN, the ALPIDE chip equipped with the AERD readout mechanism achieved a prototype readout speed of 10 MHz, with efforts underway to increase this to 40 MHz[14–18]. Similarly, the eXTP mission successfully enhanced readout speed and reduced data throughput using region of interest (ROI) readout techniques[19–21].

In pixel-level time measurement, traditional technical solutions involve various technologies based on time-to-digital converters (TDC), such as time counters[22], delay-locked loops (DLL)[23], and voltage-controlled oscillator (VCO) schemes[24], which play an important role in high-precision time measurement. For example, the TimePix4 chip combines time counter, DLL, and VCO structures, successfully achieving a time resolution of 200 ps, with a single pixel area of 55 μm × 55 μm and a power consumption of 40 μW[25, 26]. Additionally, the TDCpix chip employs DLL technology to achieve a time resolution of 97.7 ps, with a single pixel area of 300 μm × 300 μm and a power consumption of 1.44 mW[27, 28]. The TETPIX chip developed by the Institute of High Energy Physics, Chinese Academy of Sciences, uses time counter technology to reach a time resolution of 20 ns, with a single pixel area of 150 μm × 150 μm[29]. In high-density pixel arrays, balancing time measurement accuracy, power consumption, and readout efficiency is a core challenge in design. With continuous technological advancements, the increasing complexity and cost of integrating large-area pixel arrays also restrict the widespread application of new technologies.

In response to these challenges, This article presents a novel pixel detector readout scheme that combines controllable delay chain technology with a multi-directional signal propagation mechanism. By introducing adjustable delay units within each pixel, the accuracy of signal propagation can be significantly improved, allowing for precise extraction of particle localization information based on differentiated signal propagation paths. Compared to traditional unidirectional delay schemes, this multi-directional propagation structure effectively reduces the impact of timing errors on time resolution, significantly enhancing overall readout accuracy and system robustness. The contributions of this research

* This study is supported by the National Key Research and Development-Program of China (No. 2024YFE0110101,No. 2020YFE0202002) and in part by the Self-Determined Research Funds of Central China Normal University (CCNU) from the Colleges'Basic Research and Operation of Ministry of Education (MOE) under Grant 30106240154.

† Corresponding author, dongwang@ccnu.edu.cn

are mainly reflected in three aspects: First, we designed and implemented a pixel readout circuit based on controllable delay chains, achieving multi-directional signal propagation and localization by controlling the differences in the transmission path lengths of the delay units. Second, we proposed two readout configurations: one using a dual-chain scheme for forward and backward signal transmission, and the other using a four-chain configuration suitable for omnidirectional signal propagation; both configurations significantly enhance readout efficiency. Finally, two prototype chips were fabricated using TSMC 180 nm process to evaluate the proposed scheme. ASIC-I employs a four-chain scheme with a pixel array size of 3 × 3, a chip size of 1.52 mm × 1.38 mm, and a power consumption of 4.98 mW. ASIC-II uses a dual-chain scheme with a pixel array size of 1 × 6, a chip size of 1.85 mm × 1.00 mm, and a power consumption of 10.07 mW. The experimental results indicate that the solution based on controllable delay chain technology demonstrates excellent stability under different PVT (Process, Voltage, Temperature) conditions, especially regarding timing accuracy. In summary, this research provides a practical pixel detector readout circuit design scheme for high-precision timing and efficient data acquisition, and offers valuable technical references for future high-resolution detector front-end circuit design.

II. CIRCUIT IMPLEMENTATION

A. Overal Architecture

The overall design framework of the pixel detector front-end and readout circuitry is illustrated in Fig. 1, showing the key components and their interconnections. The pixel unit consists of three primary elements: a low-noise charge-sensitive amplifier (CSA), a comparator, and a controllable delay chain.

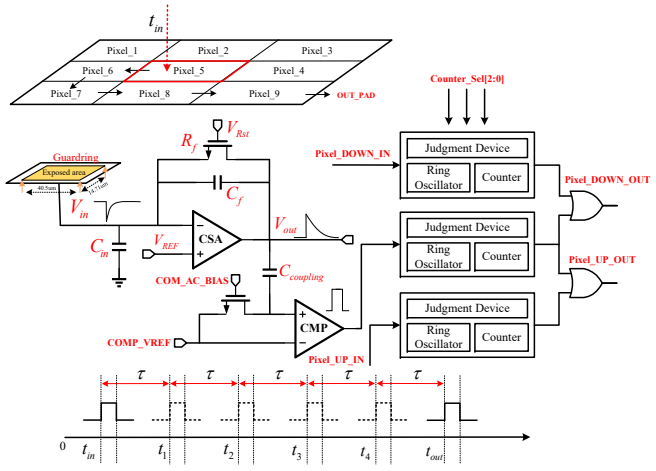

Fig. 1. Overall architecture of the pixel detector front-end and readout circuit.

In the front-end design, the top metal layer of the chip features an open-window structure, exposing the metal layer to form a electrode. When charged particles pass through, they deposit their charge on the electrode, which is subsequently fed into the CSA for signal amplification. This charge is directly proportional to the energy of the incident particles, forming the basis for precise energy measurement[30–33]. To improve testing convenience, a Guard ring is incorporated around the exposed electrode[34–37]. The primary function of the Guard ring is to couple with the electrode capacitively, allowing an excitation signal to be introduced during testing for circuit performance evaluation. Furthermore, applying a voltage to the Guard ring establishes a potential difference, creating a focused electric field around the exposed electrode to guide charges efficiently toward the collection area. This improves the efficiency of charge collection by the electrode. The design enhances the detector's sensitivity and energy resolution by leveraging an optimized electric field and efficient charge amplification, enabling more accurate measurement of the incident particle energies.

The collected charge is fed into the CSA for signal amplification. The CSA is designed with optimized transistor sizing, low-leakage feedback resistors (R_f) and capacitors (C_f) to maintain signal integrity and minimize noise. The C_f and R_f determine the amplifier's gain and time constant, providing stable and high-precision signal amplification while reducing noise through an optimized feedback network. The amplified signal is transmitted to the comparator input via a coupling capacitor (C_{coupling}). The C_{coupling} primarily eliminates the CSA baseline, ensuring stable signal processing and preventing baseline drift from affecting the comparator's sensitivity.

To further enhance performance, a bias voltage adjustment network is incorporated after the C_{coupling}. This network is composed of NMOS transistors that precisely set the baseline voltage at the node following the coupling capacitor. The adjustment aligns the signal baseline with the comparator reference voltage, ensuring that the signal remains within the comparator dynamic range. The comparator compares the amplitude of the analog signal from the CSA with a preset threshold and converts it into the corresponding digital output. This threshold is set by the comparator's internal bias network (COM_AC_BIAS) or an external reference voltage (COMP_VREF), and can be adjusted according to the amplitude detection requirements of different application scenarios. When the input signal amplitude exceeds the threshold, the comparator outputs a high-level signal; otherwise, it outputs a low-level signal. This process effectively converts the analog signal into low-jitter digital pulses, accurately triggering events and supporting high-resolution timing analysis.

The output signal from the comparator is then transmitted to a controllable delay chain, where the pulse signal undergoes delay processing. The delay chain achieves the delay operation by adjusting the oscillation period of its internal oscillator, with the number of oscillation periods adjustable via an external signal (Counter_Sel [2:0]). This flexibility allows the delay chain to meet the timing requirements of different applications, providing high temporal resolution for downstream data processing. In addition, the delay chain also utilizes the propagation characteristics of distributed delay paths. In the bidirectional propagation mode, the pulse signal generated

by the current pixel experiences a delay; at the same time, the pulse signals from the previous pixel (Pixel_DOWN_IN) and the next pixel (Pixel_UP_IN) are also processed with a controllable delay module. Each time a pulse signal passes through a pixel, it incurs a delay (τ). By analyzing the delay differences in the final output signals (Pixel_DOWN_OUT and Pixel_UP_OUT), relevant information can be extracted. This functionality not only allows for precise measurement of the arrival time of particles but also determines the hit position of the particles. As a result, the system can simultaneously acquire both spatial and temporal information of the incident particles.

B. Pixel Detector Front End

In high-precision detector systems, the quality of front-end circuit design directly impacts the overall performance of the detector. The pixel detector front-end circuit proposed in this study primarily consists of CSA and comparator, among other critical components. In this design, PMOS transistors were selected as the core components, owing to their independent N-well regions, which effectively isolate substrate noise. Compared to NMOS transistors, PMOS devices exhibit a lower 1/f noise coefficient. Consequently, the CSA employs a folded cascode structure with PMOS differential inputs, as illustrated in Fig. 2 (a).

In the circuit, transistors M1 and M2 serve as the differential input pair in the common-source configuration. Transistors M3 to M6 form the cascode current mirror, while M7 and M8 constitute the cascode stage. Transistors M9 and M10 act as current source transistors, and M11 and M12 are configured as dummy transistors. This symmetrical circuit architecture effectively suppresses common-mode noise and mitigates the impact of power supply fluctuations. The folded cascode architecture provides high output voltage gain and a larger output swing, thereby meeting the stringent performance requirements of the CSA.

However, it is noteworthy that the introduction of a differential structure increases the number of MOS devices, which could potentially lead to increased input noise. During parameter selection, the following key factors were considered: the bias current of the differential pair I_{bias1} is proportional to the transconductance of transistors M1 and M2. While a higher gain reduces the noise of the input transistors, it also increases power consumption due to the higher current. Balancing these considerations, I_{bias1} is set to 160 nA. Additionally, the bias current I_{bias2} supplied by the cascode current mirror formed by M3 to M6 is inversely proportional to the gain of the input transistors. Therefore, I_{bias2} is set to 140 nA. Finally, the bias voltages are configured as VB1 = 1 V and VB2 = 629 mV.

The comparator circuit, shown in Fig. 2(b), uses a five-transistor differential pair as the input stage, suppressing common-mode noise and enhancing sensitivity for precise amplitude discrimination. The second stage is a common-source amplifier that boosts gain, while the final inverter stage sharpens the output signal for fast digitalization. To balance power consumption, settling time, and edge response time, the bias current is set to $I_{\text{bias3}} = 120\,\text{nA}$. With an injected charge of $1\,\text{ke}^-$, the maximum transient current during the comparator's switching is 92.53 μA, with a rise time of 102.53 ps. This design achieves a favorable compromise between performance and resource constraints, ensuring reliable operation for high-performance pixel detector applications. This compact design optimizes bias currents and transistor sizes to balance precision, speed, and power, meeting single-pixel requirements in high-density detector systems.

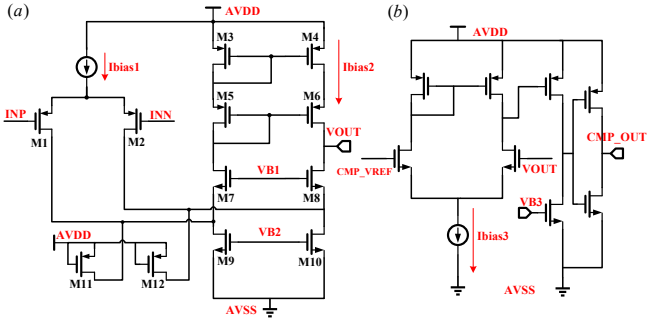

Fig. 2. (a) Schematic of the CSA front-end circuit. (b) Comparator circuit diagram.

C. In-pixel Controllable Delay Chain

The controllable delay chain is a core component of the pixel readout circuit, primarily responsible for the precise delayed transmission of pulse signals generated by pixel hit events. Through predefined transmission paths, the delay chain can extract timing information of particle hits and obtain hit position information by analyzing the delay differences between different paths. In the design, strategies involving bidirectional paths (Down and Up) and four-directional paths (Down, Up, Right, Left) are employed to enhance the system performance and flexibility. For example, in a 3 $\times$ 3 pixel array, the transmission method is shown in Fig. 3.

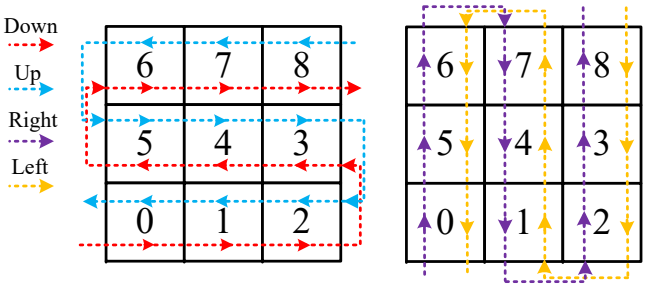

Fig. 3. Transmission direction diagram.

The structure of the controllable delay chain consists of four modules: an oscillation ring, a counter, a decision unit, and a output delay circuit, with the overall framework shown

in Fig. 4. These modules play a crucial role in the accuracy, flexibility, and reliability of the delay control mechanism. The following sections will elaborate on the working principles, functions, and performance characteristics of each sub-circuit in detail.

The oscillation ring is the basic module of the delay chain, used to generate periodic oscillation signals, with its frequency determined by the propagation time of the delay units in the loop. The oscillation ring designed here consists of a two-input NAND gate and an even number of standard delay units, with the oscillation period determined by the sum of the delay of the NAND gate and the total delay of the standard delay units. Specifically, two types of components from the digital library are used as standard delay units: CLKBUF (clock buffer) and DEL_cell (delay unit). The CLKBUF is mainly used to enhance signal driving capability, providing minimal delay while ensuring stable signal propagation; whereas DEL_cell can provide greater delay. By reasonably combining these two units, the delay parameters can be flexibly adjusted.

In this design, units *CKBD12BWP7T*(CLK12) and *DEL4BWP7T*(DEL4) are selected (the specific structure is shown in Fig. 5). Both units are based on a cascaded inverter structure, and their delay is determined by the number of inverters and the sizes of the NMOS and PMOS transistors in the inverter stages. Therefore, the oscillation period can be expressed by the following formula:

$$T = (T_{\mathrm{NAND}} + T_{\mathrm{CLK12}} \times 10) \times 2 \tag{1}$$

where T_{NAND} is the delay of the two-input NAND gate, and T_{CLK12} is the delay of each CLK12 unit.

During the optimization of design area and power consumption, the area and average current consumption of the CLK12 and DEL4 cells were measured. The simulation results show that the area of CLK12 is 12.9 μm $\times$ 4.45 μm, while the area of the DEL4 cell is 11.22 μm $\times$ 4.46 μm. At the same time, their average current consumption is 827.1 nA (CLK12) and 830 nA (DEL4), meeting the requirements for low power design.

To assess the reliability of the delay unit, we conducted simulation tests under different PVT process corners (TT, SS, FF), with the results shown in Fig. 6. Although the delay unit exhibits a high temperature coefficient under temperature variations, leading to a slight decrease in the stability of individual delay values, the overall linearity of the delay remains at a high level and is consistent across different process and temperature conditions, aligning with the expected trend.

The counter works in conjunction with the decision unit to achieve precise measurement and control of the pixel pulse signal transmission delay. The counter records the number of oscillation cycles of the oscillation ring within a preset time window and converts it into a digital value (Counter_Q [2:0]), which serves as the basis for delay control. Subsequently, the decision unit compares the counter's output with a set threshold (Counter_Sel [2:0]) to determine whether the target delay has been reached. To optimize signal processing performance, the counter output is buffered before further processing to shorten the signal conversion time and reduce timing uncertainty caused by load effects, thereby enhancing the stability and quality of signal transmission.

The output delay circuit plays a crucial role in the stable operation of the delay chain, effectively preventing the accumulation of signal delays that could lead to new input pulses occurring before the reset signal (RST_AND) has ended, which could trigger an unintended reset. To compensate for propagation time differences in the delay chain, additional delay units are introduced in the output path to ensure that the release of the reset signal precisely matches the output of the delay chain, thus maintaining the synchronization and stability of the circuit. The overall timing diagram is shown in Fig. 7.

III. TEST RESULTS

A. Experimental Setup

The purpose of this experiment is to verify the performance of the designed delay circuit chip by measuring the differences in propagation delays of signals along different paths, and to assess the measurement accuracy of the chip in obtaining particle hit time and position information during the pixel information readout process. The experiment uses a testing platform built on an FPGA main control board. The structure of the testing platform is shown in Fig. 8. The main control board generates precise and controllable pulse signals, simulating the pulse output generated by the comparator when charged particles collide with the pixels. By adjusting the time intervals between the pulse signals, it is possible to simulate particle injections at different times, thereby further studying the differences in propagation delays of signals along different transmission paths. To ensure high precision and real-time measurement of delays, the experiment selected the KEYIGHT MSO-X 4054A oscilloscope, which has a bandwidth of 500 MHz and a single-channel real-time sampling rate of 5 GSa/s (in this test, four channels are sampled simultaneously at a sampling rate of 2.5 GSa/s), allowing for high-precision capture of pulse signal delay differences of 400 ps.

This experiment designed two chips, ASIC-I and ASIC-II. ASIC-I is based on the CLKBUF delay unit, with a chip area of 1.52 mm $\times$ 1.38 mm, and extends to four transmission directions: Down, Up, Right, and Left. ASIC-II uses the DEL delay unit, with a chip area of 1.85 mm $\times$ 1.0 mm, supporting Down and Up transmission directions. Although both have the same basic working principle, ASIC-I further implements the measurement and verification of delay characteristics for multi-directional transmission paths, significantly enhancing the system's spatial resolution capability for signal propagation characteristics.

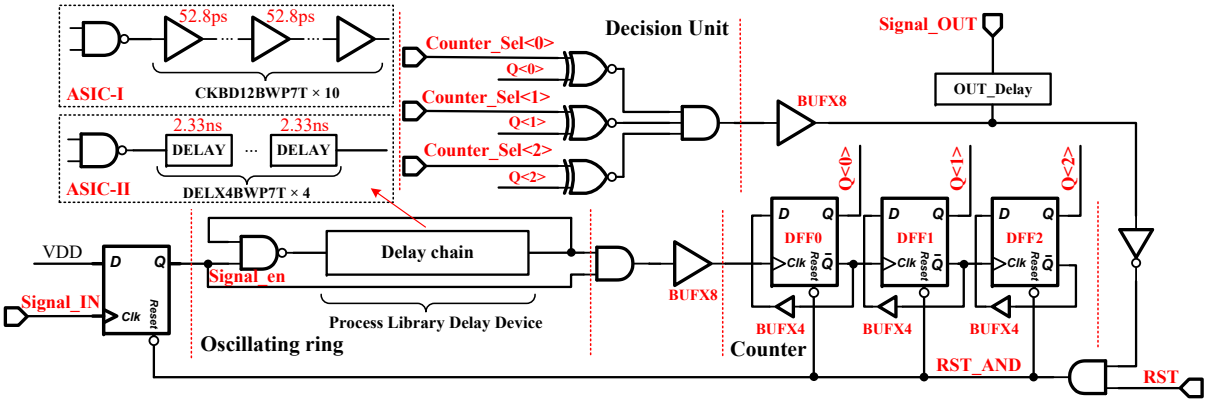

Fig. 4. Structure of in-pixel controllable delay chain.

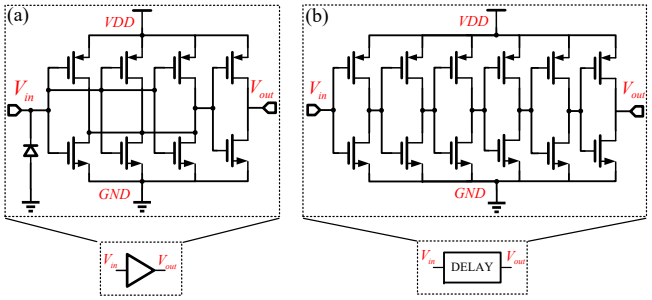

Fig. 5. (a) Circuit schematic of CKBD12BWP7T. (b) Circuit schematic of DEL4BWP7T.

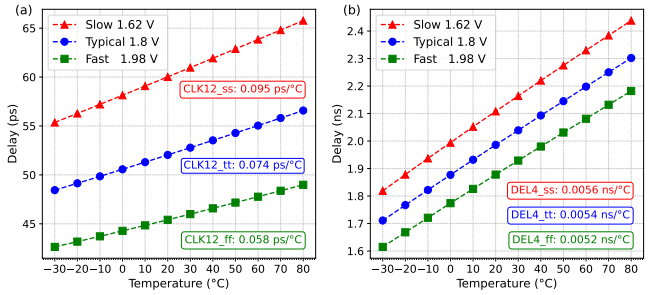

Fig. 6. (a) Delay characteristics of *CKBD12BWP7T* under different process corners. (b) Delay characteristics of *DEL4BWP7T* under different process corners. The simulation was performed with a load of 0.

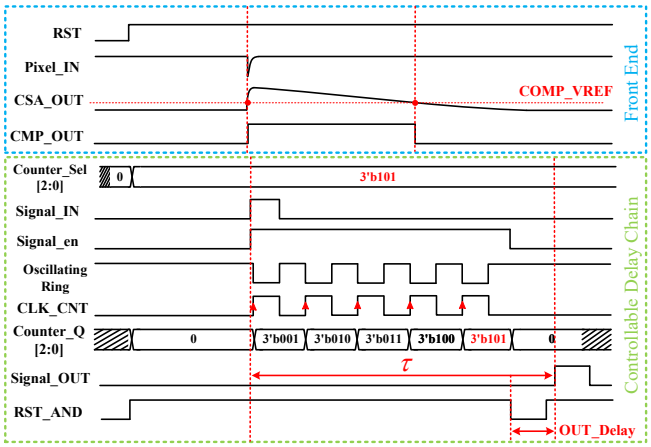

Fig. 7. Overall timing sequence of the system.

B. Results

The focus of this experiment is to conduct a quantitative analysis of the propagation characteristics of ASIC-I by measuring the delay differences along different paths to verify the stability and positioning accuracy of the designed delay circuit. The set transmission paths have been described in Section II C. As shown in Fig. 9, the oscilloscope captured the waveform data of the ASIC-I chip hitting Pixel 1. As shown in Fig. 10, the oscilloscope captured the waveform data of the ASIC-I chip simultaneously hitting Pixel 2 and Pixel 8. When a particle strikes a position within the pixel matrix, the pulse signal propagates along predefined paths to the designated output nodes. By measuring the delay differences in the vertical and horizontal directions, the precise impact position of the particle can be determined. This method utilizes the principle that the signal propagation time is proportional to the path length, achieving precise particle positioning and high-accuracy time measurement through the analysis of delay differences in multiple directions.

In the process of time statistics, due to the time sampling interval of the oscilloscope being 400 ps, this experiment performed fitting processing on the collected pulse waveforms to accurately obtain the time gap between two signals. The analysis found that the signal waveforms approximately conform to a Gaussian distribution, so we used a Gaussian function to fit the waveforms and determined the peak position of the waveforms, which corresponds to the time information of the highest point.

In the specific implementation, around the highest point of the original waveform, we took 4 points to the left and 4 points to the right, totaling 9 points for Gaussian fitting. During the fitting process, the x-coordinates of the original data were proportionally reduced to 1/10 of their original value,

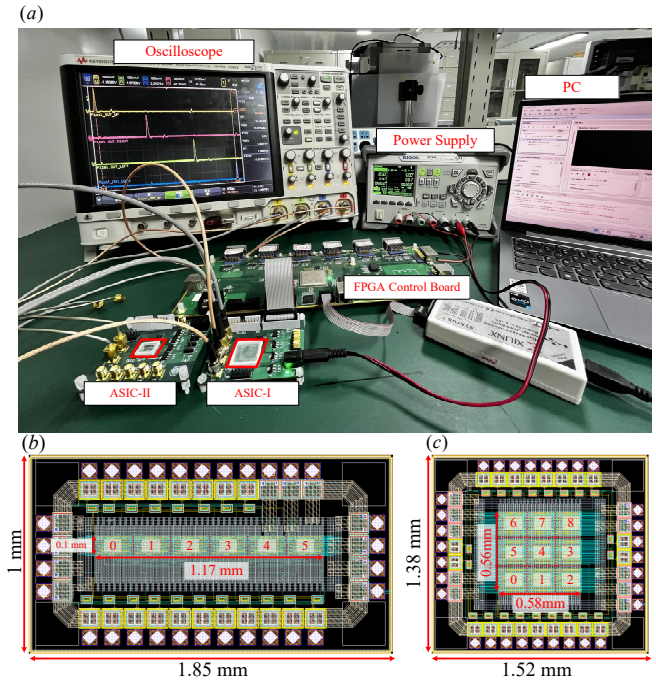

Fig. 8. Test platform. (a) Overall test platform diagram. (b) ASIC-II layout view. (c) ASIC-I layout view.

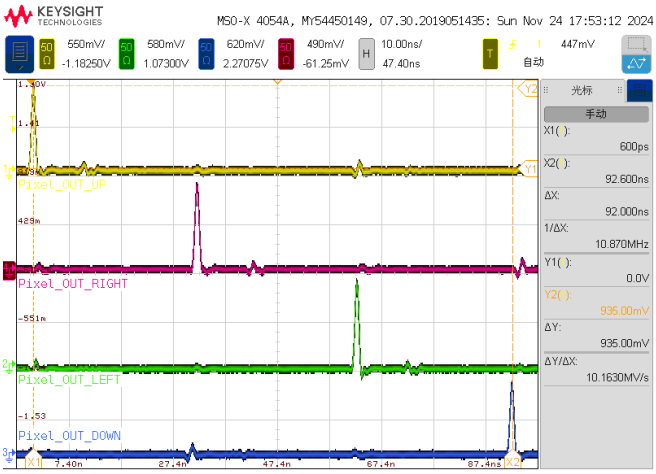

Fig. 9. Waveform capture of pixel 1 hit in multiple transmission directions. (Note: In the oscilloscope interface, the yellow, red, green, and blue traces represent the output waveforms of the Up, Right, Left, and Down transmission paths, respectively.)

thereby improving the time resolution from the sampling interval of 400 ps to 40 ps. Finally, we extracted the peak times of the two signals, t_1 and t_2, through Gaussian fitting, and calculated the time gap $\Delta t = t_2 - t_1$. This method effectively overcame the measurement errors that could arise from the limited sampling interval, significantly enhancing the accuracy and reliability of time interval measurements, and providing reliable data support for the performance verification of delay circuits. The specific implementation is shown in Fig. 11.

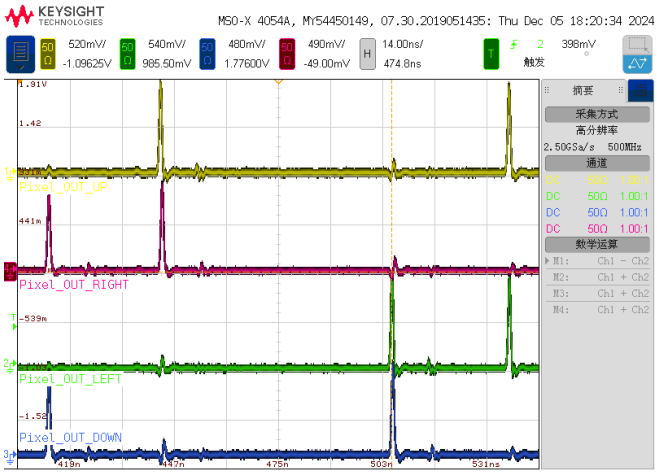

Fig. 10. Oscilloscope capture of pixel 2 and pixel 8 simultaneous hit. (Note: In the oscilloscope interface, the yellow, red, green, and blue traces represent the output waveforms of the Up, Right, Left, and Down transmission paths, respectively.)

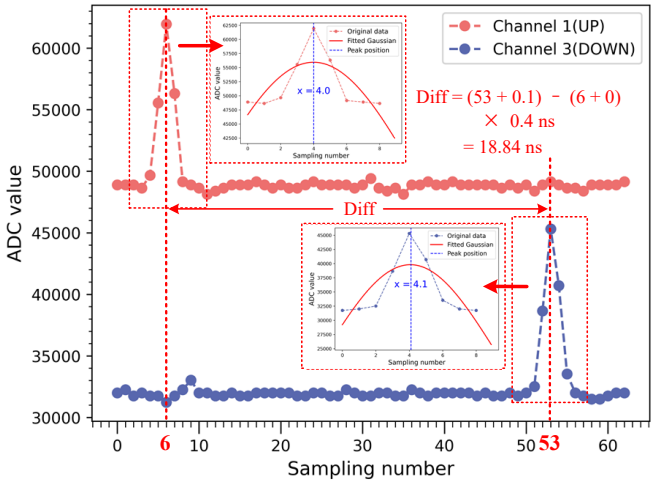

Fig. 11. Signal fitting process and time interval calculation.

Using an oscilloscope, data was collected when different pixels were hit, with each hit pixel recording 1000 frames of data. The collected data was fitted to calculate the delay difference in the Up and Down transmission directions. Figure. 12 shows the statistical distribution results of the delay differences. Meanwhile, an analysis of the delay differences in the right and left transmission directions was conducted, with the results shown in Fig. 13. The test results indicate that the system can accurately detect the delay differences of pulse signals along different paths, effectively inferring the impact position of particles. The test results are highly consistent with theoretical analysis, validating the system's high precision in acquiring positional information, with a delay measurement accuracy of about 160 ps. Performance simulations indicate that the delay precision of a single pixel reaches 108.5 ps. Additionally, the delay time exhibits excellent linearity, with nonlinear errors controlled within 0.1%, further

demonstrating the stability of the delay circuit's performance.

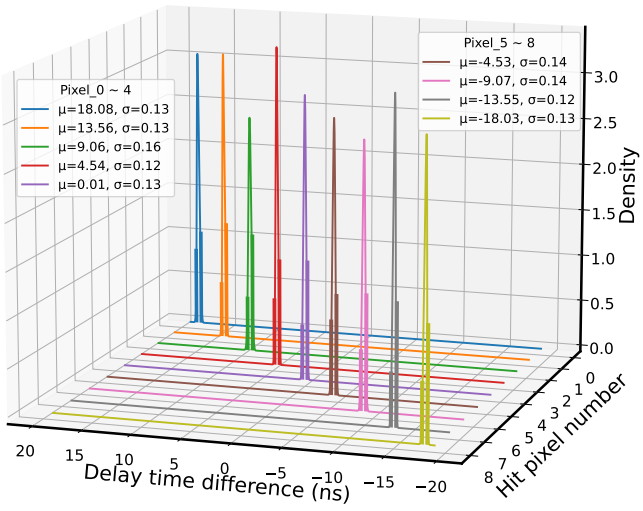

Fig. 12. Statistical distribution of delay differences in Up and Down transmission directions. (Notice: The Counter_Sel is set to 001.)

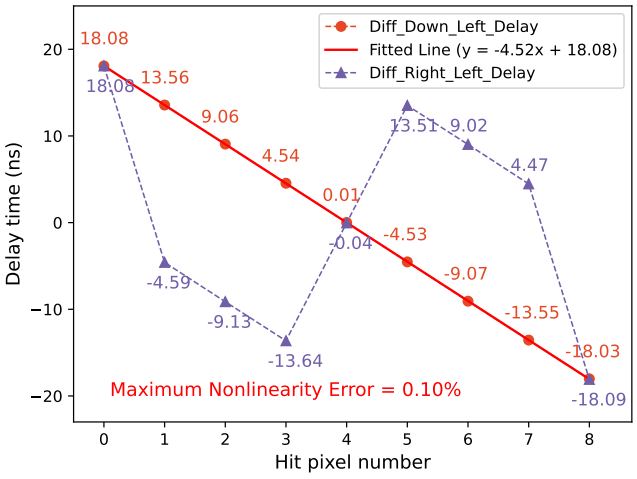

Fig. 13. Delay difference linearity of four transmission directions. (Notice: The Counter_Sel is set to 001.)

To further verify the controllable delay performance of the designed delay circuit chip, we conducted unit delay measurements for all configurations (001 to 111) by adjusting the Counter_Sel signal. The variation of Counter_Sel controls the number of cycles of the internal oscillation ring, thereby changing the delay duration of the unit delay module. During the testing process, we sequentially set Counter_Sel to 001, 010, 011, 100, 101, 110, and 111, and measured the delay differences for each configuration. At the same time, by analyzing the transmission process of different pixel hit paths, we calculated the time required for a pulse to complete one transmission within a pixel. Combining the delay configurations for all pixel hit cases, we statistically obtained the mean value of the unit time, its error range, and the corresponding current values for each configuration, as shown in Fig. 14.

The test results indicate that the delay circuit exhibits excellent response characteristics and timing accuracy under different selection signal conditions. Among them, the controllable delay range of the ASIC-I chip is from 4.55 ns to 31.1 ns, providing high timing adjustment flexibility. Although there is a slight deviation in linearity, the nonlinear error is controlled within 2.85 %, further demonstrating the high stability and adjustable accuracy of the circuit in practical applications. Under the same testing conditions, the controllable delay range of the ASIC-II chip was measured to be from 5.74 ns to 174.2 ns, significantly expanding the adjustable range.

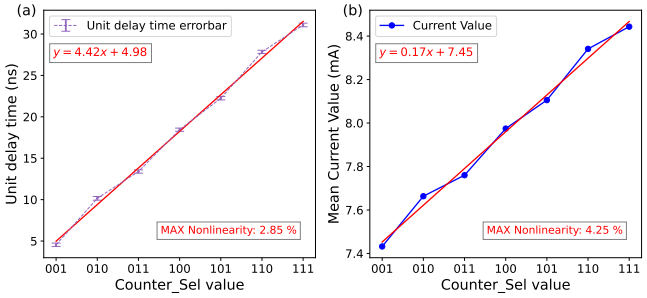

Fig. 14. Statistical analysis of unit delay mean and standard deviation for different Counter_Sel configurations. (a) Mean unit delay and error range. (b) Corresponding current values. The current refers to the current measured when the external voltage is input to the binding board.

To further verify the stability and reliability of the delay circuit, this study conducted PVT testing, taking into account the effects of different processes, voltage, and temperature conditions on delay jitter. Specifically, the study focused on the impact of temperature variations on the performance of the delay circuit. During the experiment, a high-low temperature test platform (as shown in Fig. 15) was employed, with an FPGA controlling the generation of pulse signals and adjusting the Counter_Sel size to precisely control the delay duration. The temperature range of the test platform was set from -30 °C to 80 °C, with a step size of 10 °C. Additionally, standard operating temperature data at 25 °C was also tested to simulate real-world operating conditions.

Oscilloscope measurements were taken in real time to capture the output waveforms of each transmission node under different temperature conditions, and detailed analysis was performed on the signal paths for different hit positions. For various delay configurations, the unit delay was measured under multiple temperature conditions, as shown in Fig. 16. The test results indicated that as the temperature increased, the delay also increased, which was consistent with the prior simulation results for individual components. Compared to the delay data at the standard temperature of 25 °C, the delay deviation fluctuated between 0.4 ns and 2.5 ns. Under the same delay configuration, the nonlinearity range across different temperature conditions was between 0.5 % and 0.7 %, with an overall temperature coefficient ranging from 7 ps/°C to 44 ps/°C. This comprehensive testing thoroughly assessed the dynamic response characteristics of the circuit under temper-

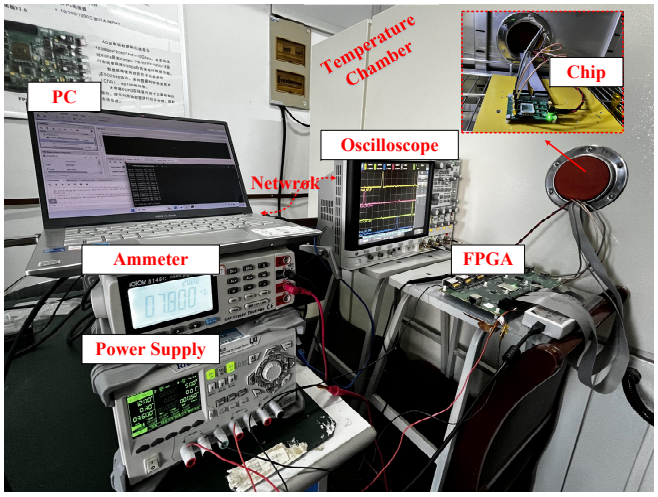

Fig. 15. High and low temperature testing platform.

ature variations and quantified the changes in delay characteristics with temperature. These results provide reliable theoretical and experimental support for enhancing the robustness and adaptability of the circuit.

IV. CONCLUSION

In this study, we present a novel pixel detector readout scheme that significantly enhances electronic readout resolution and response speed by integrating controllable delay chains within each pixel. The proposed architecture addresses key challenges of traditional pixel detectors, including limited timing resolution and susceptibility to noise, thereby improving particle detection system performance.

Experimental results validate the effectiveness of the design, achieving a timing resolution of 160 ps and a single-pixel delay unit precision of 108.5 ps. The controllable delay range spans from 4.55 ns to 31.1 ns (7 levels). Stability tests under varying PVT conditions further demonstrate the design's robustness, with a temperature coefficient ranging from 7 ps/°C to 44 ps/°C. These findings highlight the system's reliability and adaptability for diverse operational scenarios.

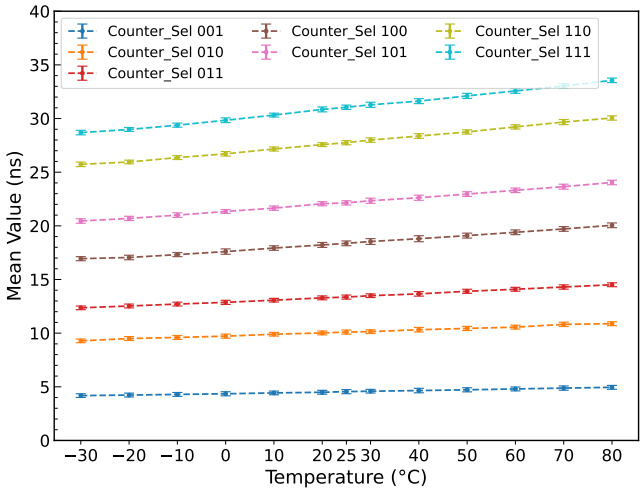

Fig. 16. Unit delay and error at different temperatures.

Furthermore, integrating advanced digital signal processing techniques within the pixel front-end establishes a scalable and modular framework for high-precision detection technologies. The proposed design not only enhances readout speed and resolution but also sets the stage for developing next-generation pixel detectors applicable to high-energy physics, medical imaging, and other advanced fields.

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